Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **CLR1**
2. **D1**
3. **N/C**
4. **PR1**
5. **Q1**
6. **N.Q1**
7. **GND**
8. **N.Q2**
9. **Q2**
10. **PR2**
11. **N/C**
12. **D2**
13. **CLR2**
14. **VCC**

**.048”**

**8**

**7**

**6**

**12 10 9**

**2 4 5**

**13**

**14**

**1**

**MASK**

**REF**

**11736B**

**.052”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: 11736B**

**APPROVED BY: DK DIE SIZE .048” X .052” DATE: 1/10/18**

**MFG: RCA THICKNESS .020” P/N: 54LS74**

**DG 10.1.2**

#### Rev B, 7/1